SPI 2025

29th IEEE WORKSHOP ON SIGNAL AND POWER INTEGRITY

PROCEEDINGS

ANGEVIN CASTLE
GAETA, ITALY
11-14 MAY

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Dear colleagues and friends,

We are delighted to present the Proceedings of the 29th edition of the IEEE Workshop on Signal and Power Integrity, SPI 2025.

It was an honor for us to once again serve as Chairs of an event that, for nearly three decades, has stood as a prominent forum for exchanging ideas on all aspects of Signal and Power Integrity — encompassing the latest research and developments in design, characterization, modeling, simulation, and testing at the chip, package, board, and system levels.

Held during May 11-14, SPI 2025 took place at the Angevin Castle's Conference Center in Gaeta, a beautiful coastal city located between Rome and Naples in central Italy, known for its pristine beaches and stunning landscapes, alongside an impressive history dating back to ancient Roman times.

The event welcomed 105 participants from 16 countries across Europe, America, and Asia. The engaging technical program featured 44 presentations in total:
— 2 tutorial talks by Prof. Grégory Houzet and Prof. Marco Donald Migliore, and 3 keynote talks by Dr. Wendem Beyene, Dr. Giovanni Frattini, and Prof. Andrea Ferrari;
— 27 oral and 9 poster presentations divided between 7 oral and 1 poster sessions;
— 3 invited talks by Dr. Tiziano Morganti, Eng. Fabio Quaglia, and Dr. Francesco Palomba during the dedicated industry panel session.

The SPI 2025 Awards & Grants were also an important feature during the workshop, aiming to encourage all participants and especially graduate students to attend the event and present their current research developments. Congratulations are due to:
— Nicola Femia, Giulia Di Capua, and Antonio Maffucci, for winning the Best Paper Award with the work titled *Power-to-Control Crosstalk in Power Electronic Circuits*;
— Antonio Carlucci, for winning the Best Student Paper Award with the work titled *An Extension of Vector Fitting to Weakly Nonlinear Circuits*;
— Antonio Carlucci and Yens Lindemans, for winning the IEEE Electronics Packaging Society's Student Travel Grants.

Complementing the scientific program, and following the workshop's established tradition, participants had the opportunity to take part in various social activities specially planned to highlight the vibrant local culture: from an enriching tour of Gaeta's Castle complemented by a delightful welcome cocktail reception to relax and network with colleagues and friends, to a wonderful exploration of the city culminating in a delicious *pizzata* dinner, ending it all with a superb gala dinner that will be undoubtedly talked about – and possibly sung – for years to come!

We would like to express our sincere appreciation to all the people, institutions and companies whose contributions were essential to make this event possible, starting with our sponsoring IEEE societies – EPS, EMCS, and MTT-S – and our private sponsors. A special mention is given to the Standing Committee members for their support and to the Technical Program Committee for their valuable work in the paper revision process. We also gratefully acknowledge our hosting institutions — the University of Cassino and Southern Lazio with the Department of Electrical and Information Engineering, and the C.R.E.A.T.E. Research Consortium. Finally, we extend our heartfelt thanks to our colleagues on the Local Committee, the technical staff, and the workshop volunteers for their indispensable assistance and dedicated efforts.

To all SPI 2025 participants, we hope you have enjoyed a successful event and a pleasant stay in Gaeta. Join us again for the next SPI workshop, to be held in May 2026 in Torino, Italy!

Antonio Maffucci, IEEE SPI 2025 Workshop Chair
Mihai Telescu, IEEE SPI 2025 Program Chair
Andrea G. Chiariello, IEEE SPI 2025 Publication Chair

IEEE ELECTRONICS PACKAGING SOCIETY Student Travel Grants

Antonio Carlucci

Politecnico di Torino, Italy

Yens Lindemans

Ghent University – imec, Belgium

IEEE SPI 2025 Best Student Paper Award

Antonio Carlucci

Politecnico di Torino, Italy

An Extension of Vector Fitting to Weakly Nonlinear Circuits

Best Paper Award

Nicola Femia [1], Giulia Di Capua [2] and Antonio Maffucci [2]

[1] University of Salerno, Italy; [2] University of Cassino and Southern Lazio, Italy

Power-to-Control Crosstalk in Power Electronic Circuits

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University of Cassino and Southern Lazio, Cassino (ITA)

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University of Brest, Brest (FRA)

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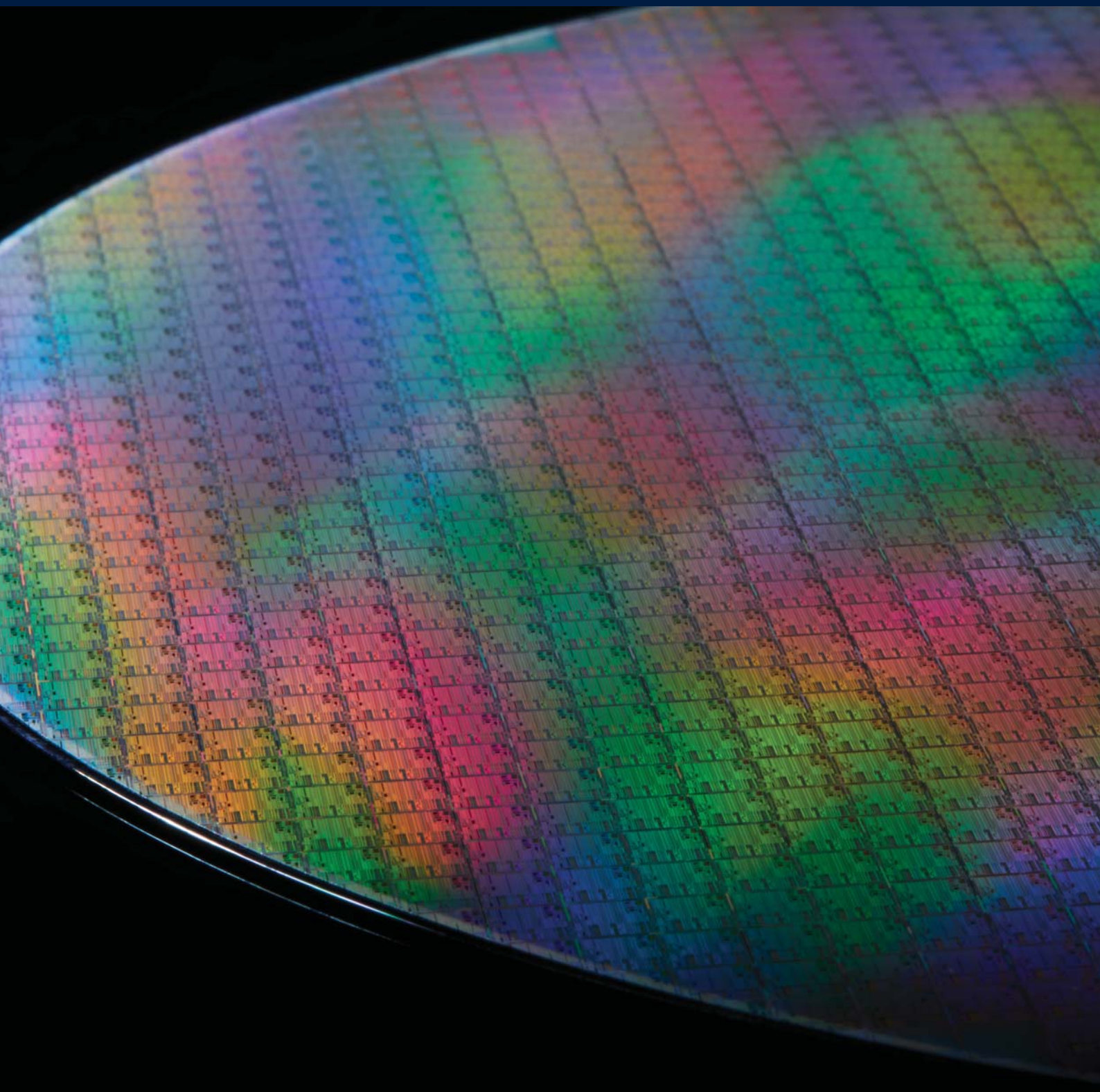

Huawei Milan Research Center

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Huawei is a Chinese multinational corporation specializing in digital communications technology. Founded in 1987, Huawei is a global leader in information and communications technology (ICT) infrastructure and smart devices. With +207,000 employees operating in more than 170 countries and regions, Huawei serves over three billion people worldwide. With 16 years of leading-edge research and +90 employees, Huawei Milan Research Center specializes in mobile communication technologies and has a strong commitment to advancing system architecture, hardware, and algorithm technologies through research and innovation.

Trends and Challenges for 5G and beyond

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Our research extends to free-space optical communications, advanced system architectures, antenna technologies, and contributions to standardization efforts. We also develop active phased array systems, focusing on innovative architectures and antenna array technologies.
Additionally, we are engaged in research on optical RFICs, including drivers and transimpedance amplifiers (TIAs), as well as microwave and millimeter-wave IC used in power amplifiers and front-end technologies.
Our research also covers HF technologies, advanced electromagnetics (EM), signal and power integrity (SPI) in next-generation high-speed systems.

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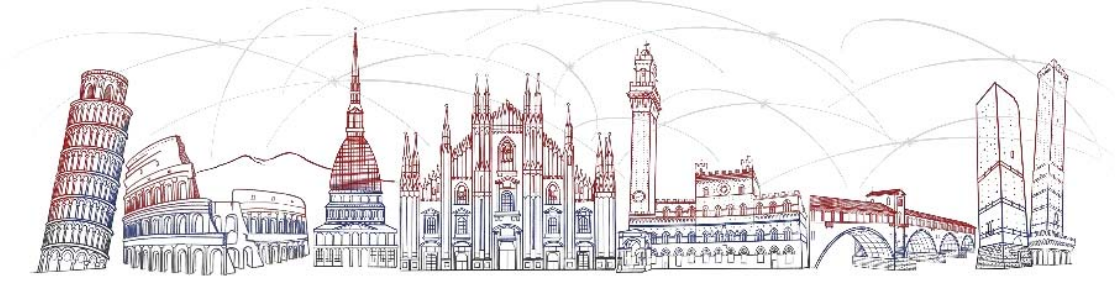

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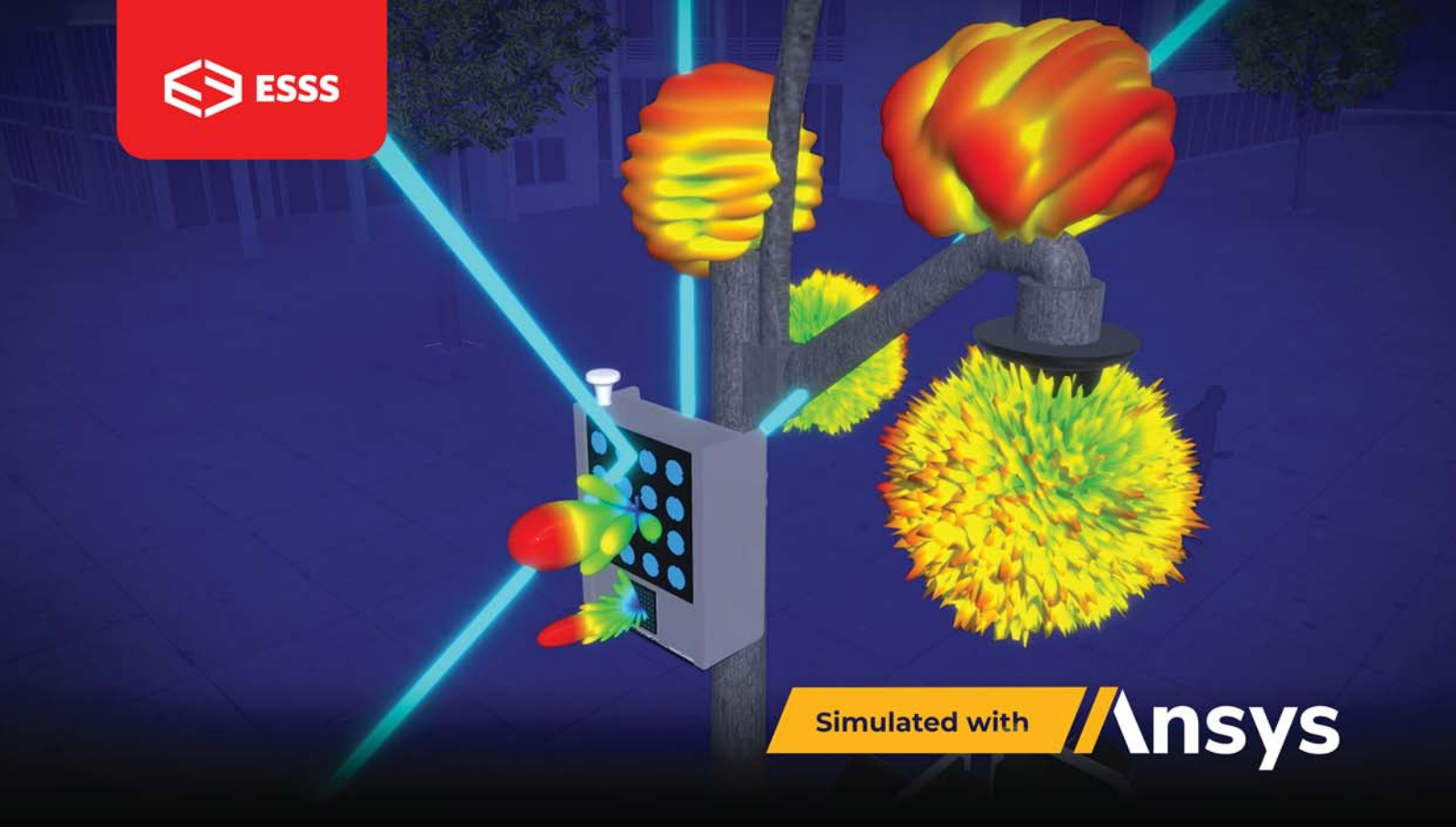

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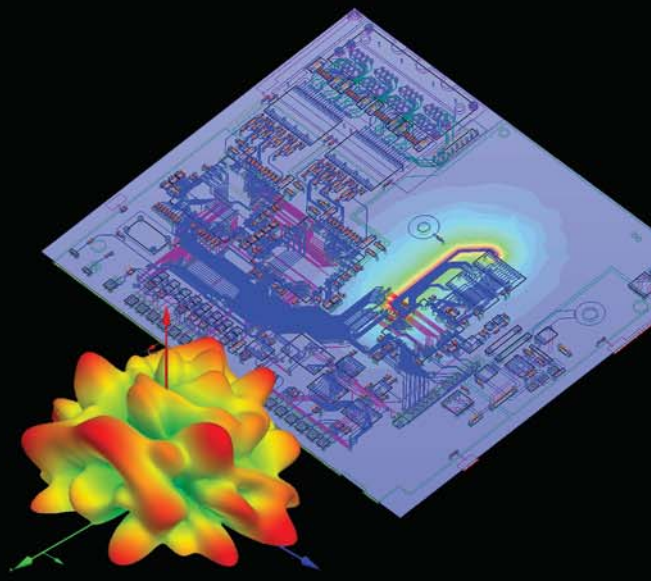

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PROGRAM AT A GLANCE

May 11, Sunday	
14:20-14:50	Registration
14:50-15:00	**Tutorials Welcome**
15:00-16:00	**TUTORIAL** **Grégory Houzet**
16:00-16:30	*Coffee-Break*
16:30-17:30	**TUTORIAL** **Marco Donald Migliore**
18:30 onwards	**Welcome Reception**

May 12, Monday	
08:30-09:00	Registration
09:00-09:20	**Opening Session**
09:20-10:00	**KEYNOTE** **Wendem Beyene**
10:00-10:40	**SESSION 1.1** **AI-Based Methods and Models**
10:40-11:10	*Coffee-Break*
11:10-12:30	**SESSION 1.2** **AI-Based Methods and Models**
12:30-14:00	*Lunch*
14:00-14:40	**KEYNOTE** **Giovanni Frattini**
14:40-15:40	**SESSION 2** **Design Optimization**
15:40-15:50	Activity IEEE TC-EDMS
15:50-16:00	Sponsor Pitch **STMicroelectronics**
16:00-16:40	**POSTER SESSION** *& Coffee-Break*
17:30 onwards	**City Tour**

May 13, Tuesday	
09:00-10:20	**SESSION 3** **Macromodeling**
10:20-10:30	Sponsor Pitch **Huawei**
10:30-10:40	Sponsor Pitch **ESSS-Ansys**
10:40-11:00	*Coffee-Break*
11:00-12:30	**INDUSTRY PANEL**
12:30-14:00	*Lunch*
14:00-14:40	**KEYNOTE** **Andrea Ferrari**
14:40-15:40	**SESSION 4** **High Speed Channels**
15:40-16:00	*Coffee-Break*
16:00-17:00	**SESSION 5** **Measurement Based Models**
18:30 onwards	**Gala Dinner**

May 14, Wednesday	
09:00-10:20	**SESSION 6** **Package Design / Power Integrity**
10:20-10:50	*Coffee-Break*
10:50-12:10	**SESSION 7** **Cross Talk & Noise Reduction / Memristors**
12:10-12:30	**Closing Session**
12:30-14:00	*Lunch*
14:00-18:00	**IBIS Summit**

14:20 – 14:50 REGISTRATION @ VENUE

Castello Angioino – Angevin Castle

GPS: 41.20754 13.58470

14:50 – 15:00 TUTORIALS WELCOME

15:00 – 16:00 TUTORIAL

High Frequency Measurements, Parameters Extraction Techniques and Microelectronic Materials Characterization

The proposed tutorial will take place through several examples of wide-band frequency characterization of materials dedicated to microelectronics. The characterization consists of extracting the relative permittivity and the loss tangent of the materials, it includes several steps which will be reviewed during the tutorial.

The tutorial will cover the following points:

1) Synthetic presentation of the different existing characterization techniques (transmission line, cavity, waveguide, etc). Selected techniques, justification of choices.
2) Presentation of the wideband frequency measurement system used: Vector Network Analyzer, coaxial cables and GSG 67 GHz and 110 GHz microwave measurement probe dedicated to microelectronics: coaxial connectivity is not suitable for connecting to microelectronic devices.
3) Quick reminder of the S parameters: reflection coefficients S11 and S22 and transmission coefficients S21 and S12.
4) Calibration of the measuring system under probes dedicated to the microwave measurement of microelectronic devices. Quick explanation of what calibration is and what it is used for; LRRM calibration will be taken as an example because it allows wide frequency band measurements. Use of specific calibration substrates.
5) Description of the test vehicles necessary for characterization: they consist of the test structure which contains the material to be characterized and the electrical connections which allow them to be connected to the measurement system.
6) Following the measurement of the S parameters of the test vehicles, presentation of the de-embedding technique which allows to extract the quantities associated only with the test structure: the ABCD parameters for instance.
7) Establishment of the electrical model of the test structure which includes the elements that are related to the electrical properties (permittivity and loss tangents) of the materials to be characterized: these are for example the parameters G (S/m or S) and C (F/m or F) of a transmission line or a capacitive device. Presentation of the process that allows these parameters to be extracted from the measurements.

8) Establishment of the relationships between the parameters of the electrical model of the test structure (G and C for example) and the relative permittivity, the loss tangent of the material to be characterized. Determination of the relative permittivity and the loss tangent.
Examples chosen to illustrate the tutorial:

a) Characterization of the "CORE" material. This material is present in multilayer substrates that allow the packaging of integrated circuits. The multilayer substrate receives the electronic chip and its encapsulation in a resin. Transmission line characterization technique. Use of conformal transformation.

b) Characterization of molding resin. The resin allows the electronic chip to be encapsulated during the integrated circuit packaging phase. Characterization method by direct contact measuring probe/material. The resin is a material that is not technologically mature, it is impossible to integrate characterization devices such as transmission lines or capacitive types.

c) Characterization of Solder Mask material. The solder mask participates in the packaging of integrated circuits. It is a thin layer that is typically applied to multilayer substrates (dedicated to packaging) to protect the copper lines from oxidation. Differential characterization technique in transmission line. Use of conformal transformation.

d) Other materials and techniques depending on the time remaining.

Grégory Houzet
Université Savoie Mont Blanc, France

In 2009, Grégory Houzet defended his Ph.D thesis at the University of Lille with a subject on the propagation of electromagnetic waves in metamaterials and the possibility of tuning these structures using ferroelectric thin films.

Since 2010, he has joined the Centre for Radiofrequencies, Optic and Micronanoelectronics in the Alps (CROMA) at the Université Savoie Mont Blanc as an associate professor. He conducts his research on high-frequency characterization techniques for dielectric materials, and more recently on antennas for telecommunications or biomedical applications.

16:00 – 16:30 COFFEE-BREAK

16:30 – 17:30 TUTORIAL

S-parameter Measurement and Calibration Techniques

Accurate S-parameter measurements of high-frequency devices using Vector Network Analyzers (VNAs) require careful correction of systematic errors. This involves the use of a suitable calibration procedure, by which the response of the measurement circuit can be effectively separated from the raw measurement data to isolate the actual response of the device. The accuracy of this calibration

process, together with the precision of the measurement procedure itself, significantly influences the final measurement uncertainty.

This tutorial introduces the theoretical basis of VNA calibration techniques and provides practical guidance on their correct implementation for high-frequency S-parameter measurements.

Topics include:

— Error Evaluation: How to analyze systematic errors in transmission and reflection measurements using signal flow graph.

— Calibration Techniques: How to reduce systematic errors in transmission measurements using calibration techniques, analyzing the advantages and critical points of the VNA calibration process.

— Practical Considerations: Some strategies for correctly implementing the calibration process and improving measurement accuracy.

— Application examples: Practical examples of microwave measurements for materials characterization.

Marco Donald Migliore

University of Cassino and Southern Lazio, Italy

Marco Donald Migliore received the Laurea (Hons.) and Ph.D. degrees in electronic engineering from the University of Naples “Federico II”, Italy . He is a Full Professor at the University of Cassino and Southern Lazio, Italy, where he also directs the Microwave Laboratory.

Professor Migliore has held visiting professorships at several international institutions, including the University of California San Diego, USA, the University of Rennes I, France, the Centria Research Center, Finland, and the Harbin Technical University, China.

His main scientific interests currently include the synthesis and characterization of antennas and high-frequency components, massive MIMO antennas and propagation, electromagnetic information theory, and medical and energetic applications of microwaves.

17:30 – 18:30	ANGEVIN CASTLE TOUR

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18:30 onwards	WELCOME RECEPTION

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08:30 – 09:00 REGISTRATION @ VENUE

09:00 – 09:20 OPENING SESSION

09:20 – 10:00 KEYNOTE

The Challenges in Signal Integrity and Power Integrity to Meet the Demands of Expanding and Evolving Compute Platforms

As compute platforms evolve from mainframes and desktops toward laptops, portable tablets, smartphones and AR/AV Devices and back to data centers (in the age of AI), the demands of signal integrity and power integrity (SI/PI) challenges have been growing and changing. The newer platforms require more complex and sometimes drastically different SI/PI analysis approaches to optimize the system performance that are specific to these platforms.

In this talk, I will start with a review of the key methods developed in the last three decades to accurately solve very complex SI/PI problems, that have now become indispensable tools in designing the most powerful compute and communication electronic systems all around us. These accomplishments have been possible with the use of techniques such as scattering parameters, recursive convolution, model order reduction, target impedance, statistical simulation etc.

Then, the SI/PI techniques were successfully used to solve the latest power distribution network challenges of current SoC chips from very low power to very large power with trillions of gates in the latest technology node as well as high-speed signaling challenges at the data rates beyond 224 Gbps were also examined. This will be followed by a brief introduction to the machine learning techniques, where the details of some of the most promising machine learning techniques applied to signal and power integrity problems are reviewed. These include machine learning techniques applied to model order reduction, target power impedance of power distribution of modern SoC, and design space exploration, to name a few.

Wendem Beyene
Reality Labs, Meta Platforms, USA

Dr. Wendem Tsegaye Beyene has been employed, in the past, by IBM, Hewlett-Packard, and Agilent Technologies, Rambus, and Intel. He is currently an Analog & Mixed Signal Architect in Reality Labs at Meta Platforms.

Dr. Beyene is an IEEE fellow, and a Senior Area Editor of IEEE CPMT and has served as a Distinguished Lecturer for IEEE EMCS as well as for IEEE EPS societies since 2020. He is also an elected Associate Fellow of the Ethiopian Academy of Sciences. Since 2022, he has organized an annual IEEE EPS and IEEE EDS sponsored conference, DTMES, in Addis Ababa, Ethiopia, with an intention of creating and boosting research in the areas of electronic design for devices, chips, packages, and systems in Ethiopia and the rest of Africa.

SESSION 1.1	
09:20 – 10:00	AI-BASED METHODS AND MODELS
	Chair: Mihai Telescu

10:00

Jose Enrique Hernandez-Bonilla (1), Torben Wendt (1), Torsten Reuschel (2), Cheng Yang (3), Christian Schuster (3)

(1) Robert Bosch GmbH, Germany; (2) University of New Brunswick, Canada; (3) Technische Universität Hamburg, Germany

Data-Driven Prediction of Temperature-Dependent Dielectric and Conductive Parameters Based On Differential Stripline Characteristics

10:20

Devi Sreekumar, Shalabh Gupta

Indian Institute of Technology Bombay, India

Efficient Synthesis and Simulation of High-Density Interconnects using Machine Learning

10:40 – 11:10 COFFEE-BREAK

SESSION 1.2	
09:20 – 10:00	AI-BASED METHODS AND MODELS
	Chair: Tom Dhaene

11:10

Marco Atlante (1), Riccardo Trinchero (1), Igor S. Stievano (1), Mihai Telescu (2), Noël Tanguy (2)

(1) Politecnico di Torino, Italy; (2) Univ. Brest, Lab-STICC, CNRS, France

SPICE-based Behavioral Models of IC Buffers via Compact Kernel Regressions

11:30

Michele Cusano (1), Riccardo Trinchero (1), Igor S. Stievano (1), Stefano Grivet-Talocia (1), Paolo Manfredi (1), Stefanie Schatt (2)

(1) Politecnico di Torino, Italy; (2) Continental Automotive Technologies GmbH, Germany

A Multi-Output Active Learning Method for the Uncertainty Quantification of PCB Lines

11:50

Til Hillebrecht, Tommy Weber, Johannes Alfert, Christian Schuster

Hamburg University of Technology, Germany

Unified Pre-Processing Steps Reducing the PCB Design Space to Enable ML Applications for Signal and Power Integrity Analysis

12:10

Ahsan Javaid, Ramachandra Achar

Carleton University, Canada

Efficient Multiconductor Transmission Line Analysis via Hybrid Deep Equilibrium NN Model

12:30 – 14:00 LUNCH

14:00 – 14:40 KEYNOTE

What Does It Take to Make an Isolated Power Converter as a System-In-Package: an IC Designer's Perspective

Integrating a complete electronic system into a single package presents both challenges and opportunities, requiring a shift in design perspective compared to traditional discrete, board-level implementations. This talk will use the example of an integrated isolated DC/DC converter to illustrate how system integration impacts circuit topology selection and key parameters. The discussion will begin with the most significant factor: switching frequency, which influences the choice of technology for the magnetic component, its design constraints, and overall performance. Additionally, electromagnetic modeling, simulation, and optimization of the entire system, including packaging and interconnections, are essential for achieving the optimal size/performance tradeoff. In these systems, all of these factors are interdependent, requiring a holistic approach to design and simulation.

Giovanni Frattini

Analog Devices, Italy

Giovanni Frattini received the M.S. degree in electronic engineering from the University of Pavia, Italy, in 1997.

In the same year he joined STMicroelectronics, Milan, Italy, as an Analog Designer in the BCD technology research and development group, where he was involved in designing signal analog circuitry for smart power chips, data converters, HV linear and dc/dc power converters. In 2008 he joined National Semiconductor (then Texas Instruments), to start and lead the Research and Development Team in the Design Center located in Milan, Italy. He served as Senior Technologist for the R&D teams in Italy and Germany for power management applications. Since 2019 he joined Analog Devices in Milan, Italy.

His current research interests include fully integrated power converters, high-voltage applications, high-frequency switching power conversion, isolated power converters and isolated gate drivers. He is author or co-author of 38 papers and holds 16 patents.

14:40 – 15:40	SESSION 2 DESIGN OPTIMIZATION Chair: Paolo Manfredi

14:40

Jordan R. Keuseman, Timothy Daun-Lindberg, Chad M. Smutzer, Clifton R. Haider

Mayo Clinic, USA

Tuning Unconventional Control Parameters for Optimal Transient Load Response in Multiphase Constant On-Time Switching Converters

15:00

Yens Lindemans, Thijs Ullrick, Ivo Couckuyt, Dirk Deschrijver, Tom Dhaene

Ghent University – imec, Belgium

Bayesian Optimization of Microwave Filters: A Physics-Informed Approach Using the Szegö Kernel

15:20

Abdullah Kayacan (1), Mustafa Gökçe Baydoğan (1), Ahmet Cemal Durgun (2), Kemal Aygün (3), Duye Ye (3), Cemil Geyik (3), Tolga Memioğlu (3)

(1) Boğaziçi University, Türkiye; (2) Middle East Technical University, Türkiye; (3) Intel Corporation, USA

Shadow Void Optimization of Microelectronic Packages with Tree-based Learners

15:40 – 15:50 IEEE TC-EDMS

Antonio Maffucci

University of Cassino and Southern Lazio, Italy

Activity of the IEEE Electrical Design, Modeling and Simulation technical committee

15:50 – 16:00 SPONSOR PITCH

STMicroelectronics, Italy

Rahul Kumar

16:00 – 16:40	POSTER SESSION	*& Coffee-Break*
	Chair: Tommaso Bradde	

P-01

Sayed Mobin, Xu Wang, Harrison Pham, Pavan Gupta, Judy Crane

Alphabet Inc, USA

Navigating the Signal Seas: Addressing MIPI C-PHY Signal Integrity Challenges in a Typical Camera Module

P-02

Hung-Chun Kuo, Po-Chih Pan, Li-Chieh Hung, Ming-Fong Jhong, Chen-Chao Wang

Advanced Semiconductor Engineering, Taiwan

Worst Eye Performance Analysis for Advanced Package Die-to-Die Interconnects

P-03

Artur D. Pescador (1), Daniel N. de Araujo (2), Stefan J. de Araujo (3), Peter Mas (4)

(1) Université Paris-Dauphine-PSL, France; (2) Siemens, USA; (3) University of Texas Austin, USA; (4) Siemens, France

Current Density Prediction Using Neural Operators

P-04

Ethan Thieme (1,2), Biliana Paskaleva (1), Xu Chen (2), Pavel Bochev (1)

(1) Sandia National Laboratories, USA; (2) University of Illinois at Urbana-Champaign, USA

A Hammerstein Approach for Compact Model of Nonlinear Circuits with Arbitrary Terminations

P-05

Rıza Arman Tosun (1), Deniz Kuzucu (1), Ahmet Cemal Durgun (1), Mustafa Gökçe Baydoğan (2)

(1) Middle East Technical University, Türkiye; (2) Boğaziçi University, Türkiye

Fine-Pitch Interconnect Modeling Using Physics-Informed Neural Networks

P-06

Khitem Lahbacha (1), Antonio Maffucci (1), Giulia Di Capua (1), Gianfranco Miele (1), Andrea Gaetano Chiariello (2), Thi Dao Pham (3), Djamel Allal (3)

(1) University of Cassino and Southern Lazio, Italy; (2) University of Campania "Luigi Vanvitelli", Italy; (3) Laboratoire National de Métrologie et d'Essais, France

Signal Integrity Analysis and Measurement of Thin Film Microstrip Lines (TFMSLs)

P-07

Ifiok Umoh (1), Adrianna Hinojosa (1), Adefisayo Adepetun (1), Benjamin Lopez (2)

(1) Intel Corporation, USA; (2) Intel Corporation, Mexico

Analysis of BGA/Socket Differential Signal Pin-Field Egress For Improved Signaling Performance

P-08

Vipul Kumar Nishad (1), Atul Kumar Nishad (2)
(1) Indian Institute of Technology Ropar, India; (2) National Institute of Technology Warangal, India

Frequency-Dependent Mutual Inductance in Broadside-Coupled Superconducting Striplines

P-09

Glauber De Freitas Lima (1), Yve Lembeye (2), Fabien Ndagijimana (3), Jean-Christophe Crebier (2)
(1) CEA, LETI, DRT, Univ. Grenoble Alpes, France; (2) Univ. Grenoble Alpes, CNRS, Grenoble INP, France; (3) Univ. Grenoble Alpes, France

Near field radiated EMI signature characterization of modular power converters based on Dual Active Bridge: from calibration to results

17:30 – 20:00	CITY TOUR

Departure from Piazza Generale Vincenzo Traniello

GPS: 41.20973 13.58388

20:00 onwards	PIZZATA DINNER

Ristorante Re Ferdinando II

GPS: 41.20968 13.58400

SESSION 3
09:00 – 10:20 MACROMODELING
Chair: Ramachandra Achar

09:00

Stefan de Araujo (1), James Pingenot (2), Daniel de Araujo (2)

(1) University of Texas Austin, USA; (2) Siemens, USA

Acyclic Connected Graph Optimization for Generative Measurement Based Models

09:20

Bijan Shahriari, Roni Khazaka

McGill University, Canada

High Order Polynomial Projection Operators for Circuit Macro-Modeling

09:40

Antonio Carlucci (1), Ion Victor Gosea (2), Stefano Grivet-Talocia (1)

(1) Politecnico di Torino, Italy; (2) Max Planck Institute for Dynamics of Complex Technical Systems, Germany

An Extension of Vector Fitting to Weakly Nonlinear Circuits

10:00

Rahul Kumar (1), Manish Bansal (1), Anil Kumar Dwivedi (1), Kirtiman Singh Rathore (1), Rhani Menzer (2)

(1) STMicroelectronics Pvt Ltd, India; (2) STMicroelectronics Pvt Ltd, France

Bridging the Gap: Correlating IBIS-AMI Simulations with Post-Silicon Measurements for a 6.25 Gbps Transmitter

10:20 – 10:30 SPONSOR PITCH

Huawei, Italy

Marco De Stefano

10:30 – 10:40 SPONSOR PITCH

ESSS-Ansys, Italy

Andrea Serra

10:40 – 11:00 COFFEE-BREAK

11:00 – 12:30 INDUSTRY PANEL

Chairs: Nicola Femia and Giulia Di Capua

11:00

Tiziano Morganti

EPC – Efficient Power Conversion, Italy

EPC GaN technology: exploiting the fastest power switch in the market

11:20

Fabio Quaglia

Analog Devices Inc., Italy

Driving and protecting GaN power switches: challenges and opportunities

11:40

Francesco Palomba

Keysight Technologies, Italy

How to add the effects of parasitics and return currents to your power converter simulations to get your circuit to work faster and more predictably

12:00

Open Discussion Panel

12:30 – 14:00 LUNCH

14:00 – 14:40 KEYNOTE

The Roadmap to Applications of Graphene and Related Materials

Graphene and layered materials have great potential in photonics and optoelectronics, where the combination of their optical and electronic properties can be fully exploited, and the absence of a bandgap in graphene can be beneficial. The linear dispersion of the Dirac electrons in graphene enables ultra-wide-band tunability as well as gate controllable third-harmonic enhancement over an ultra-broad bandwidth, paving the way for electrically tuneable broadband frequency converters for optical communications and signal processing. Saturable absorption is observed as a consequence of Pauli blocking and can be exploited for mode-locking of a variety of ultrafast and broadband lasers. Graphene integrated photonics is a platform for wafer scale manufacturing of modulators, detectors and switches for next generation datacom and telecom. These functions can be achieved with graphene layers placed on top of optical waveguides, acting as passive light-guides, thus simplifying the current technology. Heterostructures based on layers of atomic crystals have properties different from those of their individual constituents and of their three dimensional counterparts.

The combinations of such crystals in stacks can be used to design the functionalities of such heterostructures, that can be exploited in novel light emitting devices, such as single photon emitters, and tuneable light emitting diodes.

Andrea Ferrari
Cambridge Graphene Centre, University of Cambridge, UK

Andrea Ferrari is Professor of nanotechnology at the University of Cambridge and a Fellow of Pembroke College. He founded and directs the Cambridge Graphene Centre. He is a Fellow of the Royal Academy of Engineering, the American Physical Society, the Materials Research Society, the Institute of Physics, the Optical Society, the Royal Society of Chemistry, the European Academy of Sciences and the Academia Europaea, and he received numerous awards, such as the Royal Society Brian Mercer Award for Innovation, the Royal Society Wolfson Research Merit Award, the Marie Curie Excellence Award, the Philip Leverhulme Prize and the EU-40 Materials Prize.

14:40 – 15:40	SESSION 4 HIGH SPEED CHANNELS Chair: Yutaka Uematsu

14:40

Seonghi Lee, Seongho Woo, Seunghun Ryu, Sanguk Lee, Hyunwoo Kim, Jinwook Lee, Dongkyun Kim, Jiseong Kim, Seungyoung Ahn

Korea Advanced Institute of Science and Technology, Republic of Korea

A Novel Termination Resistance-Controlled Passive Equalization Method for Signal Integrity Enhancement in High-Speed Channel

15:00

Nikhita Baladari (1), Trent Uehling (2), Frank Paglia (2), Stan Cejka (2)

(1) NXP Semiconductors, Netherlands; (2) NXP Semiconductors, USA

Design and Electrical Modeling of High-Speed Interfaces in a Novel Chiplet Package

15:20

Mekala Girish Kumar (1), Yash Agrawal (2), Rohit Sharma (3)

(1) VIT-AP University, India; (2) Dhirubhai Ambani Institute of Information and Communication Technology, India; (3) Indian Institute of Technology Ropar, India

High Frequency Analysis of Cu-CNT based Tapered TSV Bumps

SESSION 5	
14:40 – 15:40	MEASUREMENT BASED MODELS
	Chair: Grégory Houzet

16:00

Luigi Ferrigno (1), Vincenzo Mottola (1), Simone Palazzo (1), Annunziata Sanseverino (1), Alessandro Sardellitti (2), Antonello Tamburrino (1,3)

(1) University of Cassino and Southern Lazio, Italy; (2) Universitas Mercatorum, Italy; (3) Michigan State University, USA

Dimensional Analysis and FPGA-Based Implementation for Real-Time Thickness and Conductivity Estimation in Eddy Current Testing

16:20

Tommaso Bradde (1), Arne Schröder (2), Dierk Bormann (3), Alexandru Savca (2), Stefano Grivet-Talocia (1)

(1) Politecnico di Torino, Italy; (2) Hitachi Energy Research, Switzerland; (3) Hitachi Energy Research, Sweden

Measurement and Modeling of Bias-Dependent Powder Cores Permeability

16:40

Simone Negri (1), Xiaokang Liu (1), Giordano Spadacini (1), Sergio A. Pignari (1), Flavia Grassi (1), Damian Halicki (2), Aurora Sanna (2)

(1) Politecnico di Milano, Italy; (2) STMicroelectronics, Italy

Characterization of miniaturized transformers at varying operating power

18:00 onwards GALA DINNER

Departure from Piazza Generale Vincenzo Traniello

GPS: 41.20973 13.58388

SESSION 6
09:00 – 10:20 PACKAGE DESIGN / POWER INTEGRITY
Chair: Riccardo Trinchero

09:00

Jun-Bae Kim, Kwangho Kim, Chang Soo Yoon , Janghoo Kim, Jeongsik Hwang , Yoo-Chang Sung, Won-Joo Yun , Seung-Jun Bae

Samsung Electronics, South Korea

Simulation-Based Analysis of Land-Side Capacitor Integration in LPDDR5 DRAM

09:20

Marco Occhiali (1), Aurora Sanna (2), Simona Cucchi (2), Georgios Korompilis (3), Cristina Somma (2), Damian Halicki (2)

(1) Ansys, Italy; (2) STMicroelectronics, Italy; (3) Ansys, Greece

Power Integrity Performance Variation Induced by Degassing Holes in BGA Packages

09:40

Steve Sandler

PICOTEST, USA

Ultra-Low PDN Impedance Measurement Using Very Short Time Domain Acquisition

10:00

José E. Schutt-Ainé (1), Patrick Goh (2), Yi Zhou (1)

(1) University of Illinois at Urbana Champaign, USA; (2) Universiti Sains Malaysia, Malaysia

Stability of VinC LIM in Power Distribution Network Analysis

10:20 – 10:50 COFFEE-BREAK

SESSION 7
10:50 – 12:10 CROSS TALK & NOISE REDUCTION / MEMRISTORS
Chair: Jose Schutt-Aine

10:50

Nicola Femia (1), Giulia Di Capua (2), Antonio Maffucci (2)

(1) University of Salerno, Italy; (2) University of Cassino and Southern Lazio, Italy

Power-to-Control Crosstalk in Power Electronic Circuits

11:10

Yutaka Uematsu
Hitachi Ltd., Japan

Hybrid-type Power-over-data-line Filters for Mode Conversion Noise Reduction

11:30

Khitem Lahbacha (1), Antonio Maffucci (1), Andrea Gaetano Chiariello (2)
(1) University of Cassino and Southern Lazio, Italy; (2) University of Campania "L. Vanvitelli", Italy

Voltage-Drop Analysis of 1R-1D Memristor Crossbar Arrays

11:50

Suyash Kushwaha (1), Chintu Bhaskara Rao (1), Shamini P R (1), Sourajeet Roy (2), Rohit Sharma (1)
(1) Indian Institute of Technology Ropar, India; (2) Indian Institute of Technology Roorkee, India

Impact of Scaling on Large Crossbar Arrays for Neuromorphic Applications

12:10 – 12:30	CLOSING SESSION
12:30 – 14:00	LUNCH
14:00 – 18:00	IBIS SUMMIT Chair: Markus Buecker

Program available online at spi-workshop.org/ibis-summit

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